REMARKS

Claims 1-75 remain in connection with the present application. Claims 1, 6, 11, 16, 21, 26, 31, 36, 41, 46, 51, 56, 61, 66, and 71 are independent. The only amendment made to the claims in the present Amendment is a non-narrowing amendment to claim 11 to correct a minor typographical error made in the previous Amendment. The amendment to claim 11 is not an amendment made for any reason related to patentability,

Personal Interview Request

Prior to submitting this Reply, Applicant contacted Examiner King on November 5, 2003 and requested the granting of a personal interview subsequent to receipt of the present Amendment. Accordingly, upon receiving this Amendment, the Examiner has agreed to contact Applicant's representative Donald J. Daley at 703-668-8000 in the Washington, DC area to arrange for a mutually convenient time to conduct a personal interview. Accordingly, Applicant's representative awaits this call from the Examiner.

Drawing Objections

The Examiner has objected to the drawings under 37 CFR 1.83(a). The Examiner alleges that the structure of the mode selection information in claims 2-5, 7-10, 12-15, 17-20, 22-25, 27-30, 32-35, 37-40, 42-45, 47-50, 52-55, 57-60, 62-65, 67-70, and 72-75 must be shown or the features cancelled from the claims. This objection is respectfully traversed. As Applicant does not believe that further drawing corrections are necessary, no further drawings corrections have been submitted.

Applicant respectfully submits that all necessary features of the invention set forth in the various claims are already illustrated in the Figures. For example, Fig. 2 illustrates exemplary embodiments of an interface including, for example, a data circuit 32, a mode selection circuit 38, and a media gate circuit 36. Thus, Fig. 2 provides exemplary structure for various corresponding elements of claim 1 for example.

Many of the various dependent claims objected to by the Examiner further clarify the types of mode selection or control information for example, as generated by a mode selection circuit such as mode selection circuit 38 of Fig. 2 for example. Although the various dependent claims set forth more specific types of information, such as that transmitted by a mode selection circuit as set forth in claim 1 for example, and thus are proper dependent claims, drawing support for their corresponding structure **is already set forth in the mode selection circuit itself** (such as mode selection circuit 38 of Fig. 2 for example). Thus, **additional drawing figures are not necessary.**

In addition, Applicant has set forth various signal diagrams concerning various types of information such as tag information for example, in Figs. 3-5. Thus, this additionally provides further exemplary drawing support for the various dependent claims of the present application. Again, no further drawings or drawing corrections are believed to be necessary.

Finally, 35 U.S.C. § 113 indicates that the Applicant shall furnish a drawing **where necessary for the understanding of the subject matter to be patented.** Applicant believes that with regard to the various dependent claims indicated by the Examiner, further drawings are not necessary to understand these various aspects of the invention. As long as the structure of the various circuits is illustrated, as is done in Fig. 2 for example, the various specific aspects of

mode selection information, tag information, etc. does not need further illustration for an adequate understanding of the application.

Accordingly, withdrawal of the Examiner's drawing objections is respectfully requested.

Claim Rejections Under 35 U.S.C. § 112

The Examiner has rejected claims 1, 6, 11, 16, 21, 26, 31, 36, 41, 46, 51, 56, 61, 66, and 71 under 35 U.S.C. § 112, first paragraph, as based on a disclosure which is allegedly not enabling. This rejection is respectfully traversed.

The Examiner alleges that the operation of the latency-independent interface is critical or essential to the practice of the invention, but is not included in the claims and is not enabled by this disclosure. The Examiner alleges that the claims do not include how to operate the interface with the claimed elements. Applicant respectfully traverses these various assertions.

Claim 1, for example, is directed to a latency-independent interface. Claim 1 sets forth various elements of the interface itself, namely the data gate circuit, data circuit, media gate circuit, mode selection circuit, and buffer attention circuit. These elements are discussed in the specification as components of the latency-independent interface, and are shown in exemplary format by elements 32, 38, 39, 36, and 34 for example and/or elements 42, 48, 49, 46, and 44 for example. The various components of the interface as well as the operation of the interface is further discussed throughout the present application, in an exemplary format, on page 6, first full paragraph wherein the media gate signal is discussed in detail, as well as page 7, at sec, wherein various components of the interface are discussed. In addition, exemplary timing diagrams are shown in Figs. 3-5, including explanations of how the interface operates in exemplary write and read operations.

Accordingly, for at least such reasons Applicant respectfully submits that claim 1, and indeed each of the independent claims, is fully supported and enabled by the present specification and drawings. Thus, withdrawal of the Examiner's rejection with regard to each of the independent claims, is respectfully requested.

Prior Art Rejections

The Examiner has rejected claims 1, 6, 11, 16, 21, 26, 31, 36, 41, 46, 51, 56, 61, 66, and 71 under 35 U.S.C. § 102(b) as being anticipated by Aoki (U.S. Patent No. 6,272,589). This rejection is respectfully traversed.

Preferred Embodiment of the Present Application

The present application, in a preferred embodiment, is directed to a latency-independent interface provided between first and second hardware components for example. In the past, as discussed in the background of the present application, data transfer between two hardware components was synchronized by read gate and write gate control signal and latency, within a R/W channel for example, created problems. Further in technologies such as iterative turbo coding for example, requiring R/W channels or RDCs with higher latencies, known interfaces were not capable of supporting higher latencies. In a preferred embodiment, the present application **discusses an interface which is capable of supporting relatively high read and/or write latencies and is thus a latency-independent interface.**

Aoki

Aoki is directed to a method and apparatus for controlling a write buffering operation for a disk drive. The method and apparatus include a read buffer area 70 wherein data read from a disk is temporarily stored; and a write buffer area 71 wherein data to be written to a disk is temporarily stored. A CPU 8 is used to monitor the amount of data in the write buffer area 71 and if the amount is decreasing, the CPU can determine the rate at which it is decreasing. The CPU can then change the storage size of the write buffer to a new size to prevent the write buffer from being empty.

Thus, Aoki is not directed to creating a latency-independent interface, but is instead directed to a system which tries to reduce latency itself by adjusting a write buffer size. As stated in Col. 2, lines 4-6, there is a trend that the write buffer becomes empty more quickly than the read buffer area. Thus, an object of the invention of Aoki is to minimize the write buffer area in accordance with the speed of transferring write data from the host system as set forth in Col. 28-31; and to monitor a change in the amount of data accumulated in the write buffer area and change the storage size of the write buffer area to a new storage size in accordance with the change monitored by the monitoring means (as set forth in Col. 2, lines 40-45 for example).

Distinctions of the Claims

The present application, set forth in claim 1 for example, is directed to a latency-independent interface including at least a media gate circuit that transmits a media gate signal. At least such a "media gate signal" limitation is not taught or suggested by Aoki.

The media gate signal of the present application is described in the first full paragraph of page 6 for example. The media gate signal is capable of replacing conventional read and write gate control signals; is capable of indicating the location of particular sectors on track media; and/or controls and is capable of being used to control data transfer between the disk and a hardware component. Through use of the media gate signal, the interface is capable of decoupling the timing of conventional read and write gate control signals with the transfer of data by replacing those signals with a media gate signal. Thus, through the use of a media gate signal, the interface is capable of supporting read and write latencies, such as those of more than a sector long for example. **No such "media gate signal" limitation is taught or suggested by Aoki.**

The Examiner alleges that the media gate circuit that transmits a media gate signal as set forth in claim 1 for example, is met by the CPU 8 of Aoki. However, as previously stated, **the CPU 8 of Aoki is involved with monitoring the write buffer area and adjusting the storage size of the write buffer area to essentially reduce latency.** It has nothing to do with the generation of a media gate signal, which can permit an interface to **support read and/or write latencies** as discussed in the present application. Thus, Applicant respectfully submits that CPU 8 cannot be a media gate circuit as claimed in claim 1. Accordingly, withdrawal of the Examiner's rejection is respectfully requested.

For at least somewhat similar reasons, Applicant respectfully submits that Aoki does not include at least the media gate circuit of claim 6; at least a first media gate circuit of claim 11; at least a media gate circuit means of claim 16; at least a media gate circuit means of claim 21; at

least a first media gate circuit means of claim 26; at least the step of transmitting a media gate signal as set forth in claim 31; at least the step of receiving a media gate signal as set forth in claim 36; at least the step of transmitting and receiving a media gate signal as set forth in claim 41; at least a transmitted media gate signal as set forth in claim 46; at least a received media gate signal as set forth in claim 51; at least a media gate signal as set forth in claim 56; at least transmitting a media gate signal as set forth in claim 61; at least receiving a media gate signal as set forth in claim 66; and at least transmitting and receiving a media gate signal as set forth in claim 71. Accordingly, withdrawal of the rejections of each of these various independent claims is respectfully requested.

Prior Art Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 2, 5, 7-10, 12-15, 17-20, 22-25, 27-30, 32-35, 37-40, 42-45, 47-50, 52-55, 57-60, 62-65, 67-70, and 72-75 under 35 U.S.C. § 103 as being unpatenable over the alleged combination of Aoki and Dunn et al. This rejection is respectfully traversed.

Initially, Applicant respectfully submits that **the Examiner has not shown any evidence of motivation** as to why one of ordinary skill in the art would be led to combine the teachings of the data processing system of Dunn et al. with the method and apparatus for controlling write buffering operation in a disk drive of Aoki. Instead, the Examiner has merely provided his own opinion. This is not evidence.

Relying on common knowledge or common sense of a person of ordinary skill in the art without any specific hint or suggestion of this in a particular reference, is not the proper standard

for reaching the conclusion of obviousness. See *In re Sang Lee, 61* USPQ 2d 1430 (Fed. Cir. 2002). The Examiner is required to specifically identify reasons why one of ordinary skill in the art would have been motivated to select and combine the reference teachings. Further, the teachings/suggestions/motivation must come from the prior art itself, the knowledge of one of ordinary skill, or in some cases the nature of the problem to be solved. Most often, the suggestion must come from the teachings of the pertinent references themselves. See *In re Dembiczak,* 50 USPQ 2d 1614 (Fed. Cir. 1999).

If the Examiner is relying on personal knowledge to support the finding of what is known in the art, the Examiner **must provide** an affidavit or declaration setting forth specific factual statements and explanation to support the finding. See 37 CFR 1.104(d)(2) and MPEP 2144.03(c). Applicant respectfully requests the Examiner to withdraw the rejection or provide such an affidavit or declaration.

Without such specific teachings or suggestions as to why one of ordinary skill in the art would be led to combine the teachings of Dunn et al. with Aoki, Applicant believes that the Examiner has failed to provide the necessary the teaching, suggestion, or motivation for combining the references. Thus, the Examiner's rejection is improper and withdrawal of the rejection is respectfully requested.

Further, a prior art reference may be considered teaching away when a person of ordinary skill, upon reading a reference, would be discouraged from following the path set out in the reference, or would be lead in a direction divergent from the path that was taken by the

Applicant. See *In re Gurley*, 31 USPQ2d 1130 (Fed. Cir. 1994). As the CPU 8 of Aoki is involved with monitoring the write buffer area and adjusting the storage size of the write buffer area **to essentially reduce latency, it actually provides a teaching away from supporting read and/or write latencies, and further teaches away from any combination with Dunn et al.**

In addition, even assuming *arguendo* that the teachings of Aoki could be combined with Dunn et al., which Applicant does not admit for at least the above mentioned reasons, Applicant respectfully submits that the teachings of Dunn et al. would not make up for at least the aforementioned deficiencies of Aoki. Thus, for the reasons previously provided with regard to each of the various independent claims in connection with the present application, Applicant respectfully submits that each of the various dependent claims of the present application are allowable over the alleged combination of Aoki and Dunn et al., even assuming *arguendo* that they could be combined. Accordingly, withdrawal of the Examiner's rejection and allowance of each of the various dependent claims in connection with the present application is earnestly solicited.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of all outstanding objections and rejections and allowance of each of claims 1-75 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

In necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

Dated: November 6, 2003

By: _____
Donald J. Daley, Reg. No. 34,313

DJD/bof

Please address all correspondence to:

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